UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,380	02/27/2004	Leendert M. Huisman	BUR920030066US1	2379

31647 7590 11/27/2006

DUGAN & DUGAN, P.C.
55 SOUTH BROADWAY
TARRYTOWN, NY 10591

EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,380	HUISMAN ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/04 and 08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The references listed in the information disclosure statement submitted on 02/27/04 have been considered by the examiner (see attached PTO-1449).

Drawings

2. The drawing (figure 1) is objected to because **labels or legends** need to be used to identify the boxes shown in the figure 1.

A proposed drawing correction or corrected drawings are required in reply to the office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Corrected drawings sheets in compliance with 37 CFR 1.121(d) are required in reply to the office action should include all the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended". If a drawing figure is to be cancelled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheet may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header so as not to obstruct any portion of the drawing figures. If the changes are not acceptable by the examiner, the applicant will be notified and informed

of any required corrective action in the next office action. The objection to the drawings will not be held in abeyance.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Title

4. The title of "Apparatus and Method for defect isolation" is so broad as to not provide any description of the inventive concept to which the claims are directed.

Abstract

5. The abstract of the disclosure is objected to because

The abstract should **not be a copy of a claim**. Correction is required. See MPEP § 608.01(b).

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The

disclosure defined by this invention," "The disclosure describes," etc. (See MPEP j 608.01(b)).

Claim objections

6. Claims **1-32** are objected to because of the following informalities:

a) The claims (1-32) are objected to because: the lines are not **indented properly** and the **font size** should be 12 instead of 16**.** Therefore, substitute the claims with proper indentation and font size (e.g. Font size should be 12 instead of 16)

b) Claims (13-17 and 22-26) recite, "adapted to" since "further adapted to" only suggests or makes optional, the term "adapted to" fails to further limit the claim. The examiner suggests: ---further configured to---

Claim Rejections - 35 USC § 112, 1st paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the ail to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims **4, 8-12, 21, 23-26** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. MPEP § 2164.08(a) states a single means claim, i.e.. where a means recitation does not appear in combination with another recited element of means, is subject to an undue breath rejection under 35 U.S.C. 112,

first paragraph. In re Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983).

a) Claim 8 recites, "a method of testing and diagnosing a scan chain comprising altering the function of scan chain flush test mode and employing the flush test mode to test and diagnose the scan chain is a single means claim.

b) Claims 4, 8-12, 21, 23-26 are rejected under 35 U.S.C. 1 12, first paragraph, as based on a disclosure which is not enabling. A definition for "**flush** test mode" critical or essential to the practice of the invention, but not included in the claims) is not enabled by the disclosure. See In re Mayhew, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Nowhere in the specification does the Applicant provide a definition for "flush test mode" and further it unclear what the term "flush"

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims **1-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over William Barnes (U.S. PN: 6,622,273) in view of Marius Hancu (U.S. PN: 4,945,536)

As per claim 1:

Barnes teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). Furthermore, Barnes teach that the scan latch circuit for a circuit having a data output and first and second outputs for test information, the scan latch circuit comprising a scan latch having first and second inputs and a control input for selecting between said first and second inputs for input to latch circuitry of said scan latch, the circuit further having first and second select signal inputs for selecting first and second test modes in which a respective one of said first and second test information is passed to said latch circuitry, wherein said data output is connected directly to one of said first and second inputs of said scan latch, and wherein said first and second outputs and said first and second select signals are connected by further circuitry to said control and said other input of said scan latch (see col. 1, lines 37-51). Further, It is noted, however, **Barnes does not explicitly detail** the aspects of " modifying the first and second test modes of the plurality of latches". **On the other hand,** Hancu in an analogous art teaches an invention relates to methods and apparatus for testing digital systems such as digital integrated circuits or systems

comprising a plurality of digital integrated circuits (see col. 1, lines 6-9). Further, Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Bane's first and second test modes of the scan latch circuit to include the operation of modifying test modes as taught by Hancu. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the method provides test generation and accumulation in a single boundary register means avoiding the need for separate test generators and accumulators and further the method permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 27-45).

As per claims 2 and 3:

Barnes in view of Hancu teach all the subject matter claimed in claim 1 including Hancu teaches linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-61). Further, Hancu teaches that algorithms (macro), computational facilities, and memory for storage of test stimulus patterns and corresponding test result patterns are required as in LSSD techniques. More

importantly, the scannable memory elements must be reconfigured (modified) after each test stimulus pattern in order to apply test stimulus patterns and to read out test result patterns, and the test stimulus patterns and test result patterns must be transmitted between external test equipment and the system under test via interconnecting cables which limit test clock operation to rates lower than the normal operating clock rate as in LSSD techniques (see col. 3, lines 3-22).

As per claim 4:

Barnes in view of Hancu teach all the subject matter claimed in claim 1 including Hancu that in use of the test apparatus in one test mode, the test access interface (300) applies a mode control signal on the mode control bus 330 to configure the boundary register (200) in scan mode and connects the serial data input terminal (350) to the serial data input line (310). The boundary register (200), which is operable as a shift register when configured in scan mode, is clocked to shift a predetermined seed pattern into the boundary register (200) to initialize the state of the boundary register (200). The test access interface applies a reset condition or other initialization sequence to the system (100) under test and to any external systems (500) connected to the system 100 via the boundary register (200) (see col. 6, last paragraph).

As per claims 5 and 6:

Barnes in view of Hancu teach all the subject matter claimed in claim 1 including Barnes teaches a circuitry of FIG. 1 is connected to memory circuitry and has three modes of operation, a normal mode in which the memory is addressed in a conventional way to provide a data output connected to terminal D, a scan mode in which data are

scanned through the memory and the output provided at the terminal (SI) and a third built-in self-test mode in which the configuration of the memory is set, together with external circuitry to cause the memory to cycle through all the possible states of the memory (see col. 2, lines 63-67 and col. 3, lines 1-4).

As per claim 7:

Barnes teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). Furthermore, Barnes teach that the scan latch circuit for a circuit having a data output and first and second outputs for test information, the scan latch circuit comprising a scan latch having first and second inputs and a control input for selecting between said first and second inputs for input to latch circuitry of said scan latch, the circuit further having first and second select signal inputs for selecting first and second test modes in which a respective one of said first and second test information is passed to said latch circuitry, wherein said data output is connected directly to one of said first and second inputs of said scan latch, and wherein said first and second outputs and said first and second select signals are connected by further circuitry to said control and said other input of said scan latch (see col. 1, lines 37-51). Further, It is noted, however, **Barnes does not explicitly detail** the aspects of " modifying the first and second test modes of the plurality of latches". **On the other**

hand, Hancu in an analogous art teaches an invention relates to methods and apparatus for testing digital systems such as digital integrated circuits or systems comprising a plurality of digital integrated circuits (see col. 1, lines 6-9). Further, Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Bane's first and second test modes of the scan latch circuit to include the operation of modifying test modes as taught by Hancu. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the method provides test generation and accumulation in a single boundary register means avoiding the need for separate test generators and accumulators and further the method permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 27-45).

As per claim 8:

Barnes teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Furthermore, Barnes teach that the scan latch circuit for a circuit having a data output and first and second outputs for test information, the scan latch circuit comprising a scan latch having first and

second inputs and a control input for selecting between said first and second inputs for input to latch circuitry of said scan latch, the circuit further having first and second select signal inputs for selecting first and second test modes in which a respective one of said first and second test information is passed to said latch circuitry, wherein said data output is connected directly to one of said first and second inputs of said scan latch, and wherein said first and second outputs and said first and second select signals are connected by further circuitry to said control and said other input of said scan latch (see col. 1, lines 37-51). Further, It is noted, however, **Barnes does not explicitly detail** the aspects of " altering or modifying and using test modes of the plurality of latches". **On the other hand,** Hancu in an analogous art teaches an invention relates to methods and apparatus for testing digital systems such as digital integrated circuits or systems comprising a plurality of digital integrated circuits (see col. 1, lines 6-9). Further, Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes to modify or alter the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Bane's first and second test modes of the scan latch circuit to include the operation of modifying or altering test modes as taught by Hancu. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the method provides test generation and accumulation in a single boundary register means avoiding the need for separate test generators and

accumulators and further the method permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 27-45).

As per claims 9-11:

Barnes in view of Hancu teach all the subject matter claimed in claim 8 including Barnes teaches a circuitry of FIG. 1 is connected to memory circuitry and has three modes of operation, a normal mode in which the memory is addressed in a conventional way to provide a data output connected to terminal D, a scan mode in which data are scanned through the memory and the output provided at the terminal (SI) and a third built-in self-test mode in which the configuration of the memory is set, together with external circuitry to cause the memory to cycle through all the possible states of the memory (see col. 2, lines 63-67 and col. 3, lines 1-4).

As per claim 12:

Barnes teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). Furthermore, Barnes teach that the scan latch circuit for a circuit having a data output and first and second outputs for test information, the scan latch circuit comprising a scan latch having first and second inputs and a control input for selecting between said first and second inputs for input to latch

circuitry of said scan latch, the circuit further having first and second select signal inputs for selecting first and second test modes in which a respective one of said first and second test information is passed to said latch circuitry, wherein said data output is connected directly to one of said first and second inputs of said scan latch, and wherein said first and second outputs and said first and second select signals are connected by further circuitry to said control and said other input of said scan latch (see col. 1, lines 37-51). Further, It is noted, however, **Barnes does not explicitly detail** the aspects of " modifying the first and second test modes of the plurality of latches". **On the other hand,** Hancu in an analogous art teaches an invention relates to methods and apparatus for testing digital systems such as digital integrated circuits or systems comprising a plurality of digital integrated circuits (see col. 1, lines 6-9). Further, Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Bane's first and second test modes of the scan latch circuit to include the operation of modifying test modes as taught by Hancu. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the method provides test generation and accumulation in a single boundary register means avoiding the need for separate test generators and accumulators and further the method permit testing of the digital system

in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 27-45).

As per claim 13:

Barnes in view of Hancu teach all the subject matter claimed in claim 12 including Hancu that in use of the test apparatus in one test mode, the test access interface (300) applies a mode control signal on the mode control bus 330 to configure the boundary register (200) in scan mode and connects the serial data input terminal (350) to the serial data input line (310). The boundary register (200), which is operable as a shift register when configured in scan mode, is clocked to shift a predetermined seed pattern into the boundary register (200) to initialize the state of the boundary register (200). The test access interface applies a reset condition or other initialization sequence to the system (100) under test and to any external systems (500) connected to the system 100 via the boundary register (200) (see col. 6, last paragraph).

As per claim 14:

Barnes in view of Hancu teach all the subject matter claimed in claim 12 including Hancu teaches linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-61). Further, Hancu teaches that algorithms (macro), computational facilities, and memory for storage of test stimulus patterns and corresponding test result patterns are required as in LSSD techniques. More importantly, the scannable memory elements must be reconfigured (modified) after

each test stimulus pattern in order to apply test stimulus patterns and to read out test result patterns, and the test stimulus patterns and test result patterns must be transmitted between external test equipment and the system under test via interconnecting cables which limit test clock operation to rates lower than the normal operating clock rate as in LSSD techniques (see col. 3, lines 3-22).

As per claim 15:

Barnes in view of Hancu teach all the subject matter claimed in claim 12 including Hancu that in use of the test apparatus in one test mode, the test access interface (300) applies a mode control signal on the mode control bus 330 to configure the boundary register (200) in scan mode and connects the serial data input terminal (350) to the serial data input line (310). The boundary register (200), which is operable as a shift register when configured in scan mode, is clocked to shift a predetermined seed pattern into the boundary register (200) to initialize the state of the boundary register (200). The test access interface applies a reset condition or other initialization sequence to the system (100) under test and to any external systems (500) connected to the system 100 via the boundary register (200) (see col. 6, last paragraph).

As per claim 16:

Barnes in view of Hancu teach all the subject matter claimed in claim 12 including Barnes teaches a circuitry of FIG. 1 is connected to memory circuitry and has three modes of operation, a normal mode in which the memory is addressed in a conventional way to provide a data output connected to terminal D, a scan mode in which data are scanned through the memory and the output provided at the terminal

(SI) and a third built-in self-test mode in which the configuration of the memory is set, together with external circuitry to cause the memory to cycle through all the possible states of the memory (see col. 2, lines 63-67 and col. 3, lines 1-4).

As per claims 17-19:

Barnes in view of Hancu teach all the subject matter claimed in claim 12 including Hancu that in use of the test apparatus in one test mode, the test access interface (300) applies a mode control signal on the mode control bus 330 to configure the boundary register (200) in scan mode and connects the serial data input terminal (350) to the serial data input line (310). The boundary register (200), which is operable as a **shift register (scan chains)** when configured in scan mode, is clocked to shift a predetermined seed pattern into the boundary register (200) to initialize the state of the boundary register (200). The test access interface applies a reset condition or other initialization sequence to the system (100) under test and to any external systems (500) connected to the system 100 via the boundary register (200) (see col. 6, last paragraph).

As per claim 20:

Barnes teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Barnes teaches a method and apparatus permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 40-45). Furthermore, Barnes teach that the

scan latch circuit for a circuit having a data output and first and second outputs for test information, the scan latch circuit comprising a scan latch having first and second inputs and a control input for selecting between said first and second inputs for input to latch circuitry of said scan latch, the circuit further having first and second select signal inputs for selecting first and second test modes in which a respective one of said first and second test information is passed to said latch circuitry, wherein said data output is connected directly to one of said first and second inputs of said scan latch, and wherein said first and second outputs and said first and second select signals are connected by further circuitry to said control and said other input of said scan latch (see col. 1, lines 37-51). Further, It is noted, however, **Barnes does not explicitly detail** the aspects of " modifying the first and second test modes of the plurality of latches". **On the other hand,** Hancu in an analogous art teaches an invention relates to methods and apparatus for testing digital systems such as digital integrated circuits or systems comprising a plurality of digital integrated circuits (see col. 1, lines 6-9). Further, Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes (first and second test modes) to modify the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Bane's first and second test modes of the scan latch circuit to include the operation of modifying test modes as taught by Hancu. **This modification** would have been obvious because a person having ordinary skill in the art would have

been motivated to do so because the method provides test generation and accumulation in a single boundary register means avoiding the need for separate test generators and accumulators and further the method permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 27-45).

As per claim 21:

Barnes teach or disclose a scan latch circuit useable where alternative testing methods are employed on an associated circuit, and to the combination of such a scan latch circuit with an associated circuit (see col. 1, lines 1-9). Furthermore, Barnes teach that the scan latch circuit for a circuit having a data output and first and second outputs for test information, the scan latch circuit comprising a scan latch having first and second inputs and a control input for selecting between said first and second inputs for input to latch circuitry of said scan latch, the circuit further having first and second select signal inputs for selecting first and second test modes in which a respective one of said first and second test information is passed to said latch circuitry, wherein said data output is connected directly to one of said first and second inputs of said scan latch, and wherein said first and second outputs and said first and second select signals are connected by further circuitry to said control and said other input of said scan latch (see col. 1, lines 37-51). Further, It is noted, however, **Barnes does not explicitly detail** the aspects of " altering or modifying and using test modes of the plurality of latches". **On the other hand,** Hancu in an analogous art teaches an invention relates to methods and apparatus for testing digital systems such as digital integrated circuits or systems

comprising a plurality of digital integrated circuits (see col. 1, lines 6-9). Further, Hancu teaches that linear feedback paths may be provided between selected cells of the boundary register (200) in certain test modes to modify or alter the generation and accumulation characteristics of the boundary register (200) in those test modes (see col. 13, lines 58-62). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Bane's first and second test modes of the scan latch circuit to include the operation of modifying or altering test modes as taught by Hancu. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the method provides test generation and accumulation in a single boundary register means avoiding the need for separate test generators and accumulators and further the method permit testing of the digital system in isolation, testing of interconnections between digital systems and combined testing of the digital system and its connections to other digital systems (see col. 5, lines 27-45).

As per claims 22-26:

Barnes in view of Hancu teach all the subject matter claimed in claim 21 including Barnes teaches a circuitry of FIG. 1 is connected to memory circuitry and has three modes of operation, a normal mode in which the memory is addressed in a conventional way to provide a data output connected to terminal D, a scan mode in which data are scanned through the memory and the output provided at the terminal (SI) and a third built-in self-test mode in which the configuration of the memory is set,

together with external circuitry to cause the memory to cycle through all the possible states of the memory (see col. 2, lines 63-67 and col. 3, lines 1-4).

As per claims 27-32:

Barnes in view of Hancu teach all the subject matter claimed in claims 1, 7, 8, 12, 20, and 21 including Hancu the scannable memory elements have a serial or scan mode in which they are decoupled from the combinational logic and connected in series to form a shift register. Such partitioning and provision of scannable memory elements is known as Level Sensitive Scan Design (LSSD) and digital systems employing LSSD are tested by configuring the scannable memory elements in serial mode, shifting a known test stimulus pattern into the shift register, reconfiguring the scannable memory elements into parallel mode, running the system clock through a single clock cycle, reconfiguring the scannable memory elements into serial mode, and shifting a test result pattern out of the shift register (see col. 1, lines 20-33).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 5,784,382 Byers et al.

US PN: 5,617,430 Angelotti et al.

US PN: 6,223,312 Nozuyama, Yasuyuki

US PN: 5,032,783 Hwang et al.

11. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100